Factsheet
I3C Protocol®

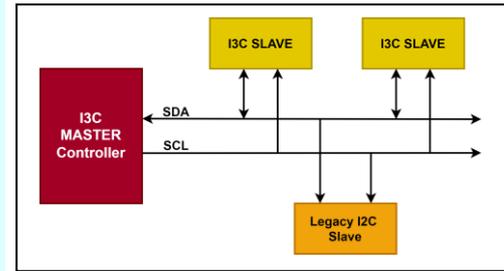# Silicon Cores™
Core to the Intelligent System™

Function Controller

Silicon Interfaces

The i3c protocol, short for "Improved Inter-Integrated Circuit," is a communication protocol designed to improve upon the widely-used I2C protocol. It was developed by the MIPI Alliance, a global organization that aims to develop interface specifications for mobile devices.

The i3c protocol includes several key features that make it an improvement over I2C. For example, it supports higher data speed, around 12.5MHz, which allows for faster communication between devices. It also includes dynamic address assignment, which allows devices to be added or removed from the bus without disrupting the communication of other devices.

Another feature of i3c is its support for both Legacy I2C slaves and I3C slave devices, which makes it compatible with a wide range of existing hardware. Additionally, it includes support for advanced features such as sensor fusion, which allows multiple sensors to be combined to provide more accurate data.
In addition to the features mentioned earlier, the i3c protocol also includes support for low-power modes, which can help conserve battery life in mobile devices. It also includes enhanced error detection and correction capabilities, which can help ensure the reliability of data transmission.

Product Specifications

- RTL Design (System Verilog).
- Test Bench (Universal Verification Methodology (UVM))
- Clock Frequency: 12MHz
- Modes: Singular Data Rate messaging (SDR).
  High Data Rate Mode Double Data Rate (HDR-DDR).
  HDR Ternary Symbol Pure-bus (HDR-TSP).
  HDR Ternary Symbol Legacy-inclusive-bus (HDR-TSL).
- Compatible with 8 bit Micro-controller.

Options:

Adaptations:
√ Generic 8-Bit 8051 Microcontroller Interface available
√ PCI/AXI possible

Add-ons:
√ Verification IP – UVM VIP

Product Highlights

- ☑ Two wire serial interface up to 12.5 MHz.
- ☑ Legacy I2C Device co-existence on the same bus.
- ☑ Dynamic Addressing while supporting Static Addressing for Legacy I2C Devices.
- ☑ Legacy I2C Messaging with the I2C protocol frame format possible.
- ☑ I2C-like Single Data Rate messaging (SDR).
- ☑ Optional High Data Rate messaging Modes (HDR) such as HDR-DDR, HDR-TSP, HDR-TSL.
- ☑ Multi-Drop capability.
- ☑ Multi-Master capability.
- ☑ In-Band Interrupt support.
- ☑ Hot-Join support.
- ☑ Synchronous Timing Support.
- ☑ Asynchronous Time Stamping.
- ☑ Protocol is robust in terms of data bytes transfer.
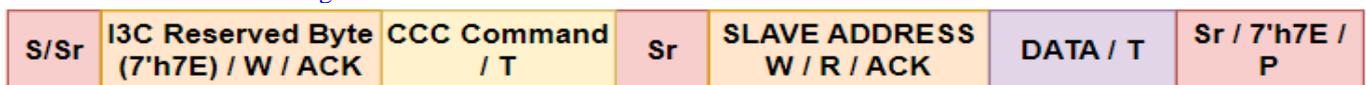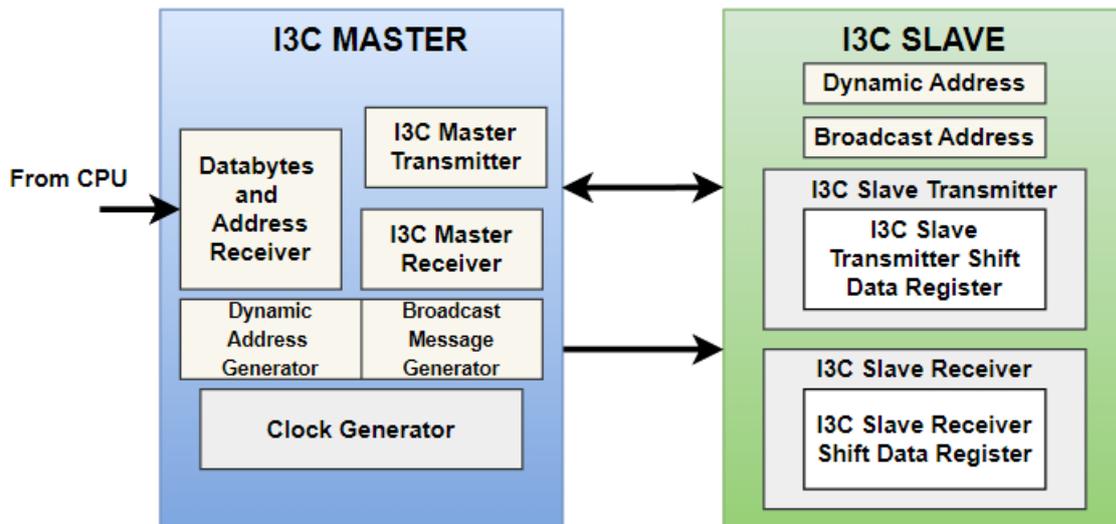

Fig. Broadcast CCC Format

Fig. Direct CCC Format

S – Start, Sr – Repeated Start, W – Write, R – Read, CCC – Common Command Code, T – Transition Bit, ACK – Acknowledge, P - Stop

I3C Protocol Block Representative

The I3C Protocol core consists of 3 modules: I3C Master Module, Legacy I2C Slave Module and I3C Slave Module.

- I3C Master Module: I3C Master module is responsible to generate the Serial Clock. Also, it is responsible to broadcast the messages to all the connected I3C Slaves which should have a default broadcast address as 7'h7E. I3C Master slave is responsible to allocate the dynamic addresses to the I3C slaves connected on the bus, also it is capable of Hot-Join which makes it possible for any slave to connect to the bus midway. Also, the I3C Master is capable to communicate with the legacy I2C Slaves with the legacy I2C messaging format (With some limitations).

- Legacy I2C Slave Module: As we know that I3C protocol supports both I3C Slaves and legacy I2C slaves on a same bus. Legacy I2C slaves runs on the pre-determine speed modes such as 100kbps, 400kbps, 1Mbps, 3.1Mbps etc. Legacy I2C slaves support only the I2C frame format for messaging. It can't be a part of message broadcasting which is one of the features I3C protocol. Also, it can't be Hot-Joined as it has a local address prior joining the bus.

- I3C Slave Module: I3C Slaves don't have a local pre-determined address; it gets its address dynamically set by the Master itself. As it supports dynamic addressing, it can be Hot-Joined into the bus at any moment. I3C Slaves has a default broadcast address of 7'h7E which is used to receive broadcasted message from the Master Controller. I3C Slaves operates on a frequency of 12.5Mhz. The packet format of I3C communication is different than the legacy I2C slaves.

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