Factsheet

PCIe3.0® - SI23PCIe30

Silicon Cores™

Core to the Intelligent System™

SI23 PCI EXPRESS

Function Controller

Silicon Interfaces' PCIe 3.0 (Peripheral Component Interconnect Express 3.0) is a computer hardware interface standard that is used to connect various components to a computer's motherboard. It is the third generation of the PCIe standard and offers increased bandwidth, improved performance, and reduced power consumption compared to its predecessor, PCIe 2.0. Overall, PCIe 3.0 provides faster and more efficient communication between the various components in a computer, including graphics cards, network adapters, and storage devices, resulting in better overall performance.

PCIe 3.0 is a high-speed, bidirectional, and low-cost point-to-point interface that is widely used in PC, consumer electronics, and mobile architectures. It supports dynamic attachment of multiple peripherals to the host via a switch or a bridge. PCIe 3.0 is an open architecture that offers higher data throughput and enables the connection of up to 128 devices to a single port on the motherboard. It is a serial protocol and physical link that transmits data differentially on multiple pairs of wires, while simultaneously providing power to the connected peripherals.

As technology advances, new types of devices, media formats, and storage systems require more bus bandwidth to deliver the desired user experience. In addition, user applications demand faster and more efficient connections between the PC and these increasingly sophisticated peripherals. PCIe 3.0 addresses these requirements by delivering a significantly higher transfer rate that matches the needs of modern usage scenarios and devices. Its increased bandwidth and other features make it an ideal interface standard for meeting the performance demands of modern computer systems.

Product Specifications

- Fully synthesizable Register Transfer Level (RTL) SystemVerilog HDL core
- Test Bench. Environment Variable: SystemVerilog
- Methodologies-based Test Bench: UVM
- Fault Simulation done
- Test Realization in Portable Stimulus Standards (PSS)
- Targeted to Synopsys® Zebu® EP-1

Options:

(May be separately priced)

Adaptations:

√ 8-Bit 8051 Microcontroller Interface available

√ 16/32-Bit Standard Microcontroller Interface available

√ DMA Functionality possible

Add-ons:

√ Verification IP – UVM VIP

Product Highlights

- ☑ Data transfer rate : PCIe 3.0 supports a data transfer rate of up-to 8 GT/s (gigatransfers per second), which is twice the speed of 2.0.
- ☑ Link width: The link width for PCIe 3.0 is up to 16 lanes, which provides a maximum bandwidth of 15.75 GB/s (gigabytes per second) in each direction.
- ☑ Lane configuration: PCIe 3.0 has the same lane configuration as its predecessor, PCIe 2.0, with up to 16 lanes. Each lane can provide up to 985 MB/s of bandwidth.
- ☑ Increased lane flexibility: PCIe 3.0 also offers increased lane flexibility, allowing the configuration of lanes to be changed dynamically depending on the needs of the system.
- ☑ Backward compatibility : PCIe 3.0 is backward compatible with PCIe 2.0 and PCIe 1.0, meaning that devices designed for earlier PCIe versions can be used with a PCIe 3.0 slot, but at a reduced speed.
- ☑ Multi-function support: PCIe 3.0 supports multi-function devices, which can provide multiple functions through a single physical device, reducing the need for multiple expansion slots.
- ☑ Power consumption : PCIe 3.0 is designed to be more power-efficient than its predecessors, which can help to reduce energy consumption and heat generation.

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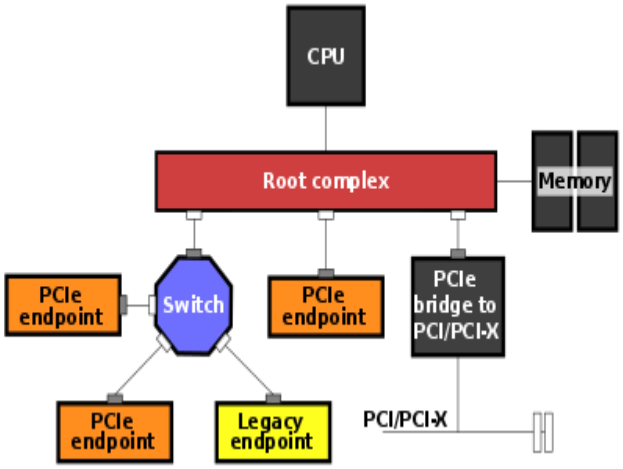
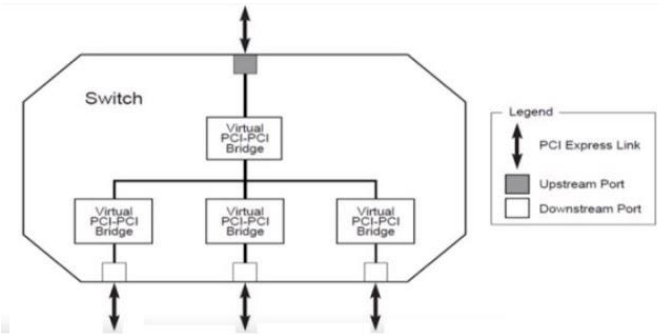
PCIe3.0 Schematic Block Representative





The block diagram depicts the basic topology of PCIe protocol consisting of Root Complex (RC), multiple Endpoints (I/O devices), a Switch, and a PCI Express to PCI/PCI-X Bridge. PCIe enables point to point connections called as links. Each link can support 1 to 32 lanes and each lane consist of 2 pairs of wires, one for transmitting and another for receiving. PCIe implementation can vary depending upon the use cases. It can be used to connect Ethernet cards, solid state devices, video cards and sound cards.

- Root complex: The interface between the system CPU, memory, and the rest of the PCIe interface. The main function of root complex is to accomplish the location conversion from the memory domain to the Pcie bus domain.
- Bridge: Provides an interface to other buses (PCI, PCI-X). Also known as a “Forward Bridge” which allows an old PCI, PCI-X card to be plugged into a new system. The opposite is called “Reverse Bridge” which allows new PCI, PCI-X cards to be plugged into old systems
- Switch: Provides expansion and aggregation capabilities, allowing more devices to be connected to a single PCIe port. Acts as a router, recognizing which path to take based on address or routing information.
- Endpoint: The end point of the Pcie bus system topology. e.g., PCIe interfaced NIC devices, hard disk devices, I/O devices.

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