	Month 1							
	Day	Week 1		Week 2		Week 3		Week 4	
		10:30 - 12:30	6:00 - 8:00 pm	10:30 - 12:30	6:00 - 8:00 pm	10:30 - 12:30	6:00 - 8:00 pm	10:30 - 12:30	6:00 - 8:00 pm
Logic Design	Day 1	- Combinational	- Combinational	Combinational - Revise	Test-Combinational	- Memory	Memory	System Design	SD - Top Down Meth
	Day 2	- Combinational	- Combinational	- Synchronous	- Synchronous	- Clocks	- Finite State	SD -Block / Flow Charts / S	Methodologies - Design
	Day 3	- Combinational	- Combinational	- Asynchronous	- Asynchronous	- Finite State	- Finite State	Meth - Verification	Documentation
	Day 4	- Sequential	- Sequential	Revise-Seq / Sync / Async	Test-Seq / Sync / Asyn	Revise-Mem / Clk / FS	Test - Mem / Clk / FS	Revise - SD	Test-SD
Environments	Day 5	Linux - Basics	Linux - Commands	Revise - Linux	Test - Linux	Scripting - Perl	Scripting -Perl	EDA flow - Frontend	EDA flow - Backend
Environments	Day 6	Linux - Commands	Linux - Src control	Scripting	Scripting - Shell	Revise - Scripting	Test - Scripting	Install - Linux	Install - Tools

	Month 2							
	Day	Week 1		Week 2		Week 3		Week 4	
		10:30 - 12:30	6:00 - 8:00 pm	10:30 - 12:30	6:00 - 8:00 pm	10:30 - 12:30	6:00 - 8:00 pm	10:30 - 12:30	6:00 - 8:00 pm
HDL	Day 1	HDL & HVL (Test Bench) - Verilog		HDL - Advanced - Verilog		HDL-Advanced - VHDL		HDL - Advanced - PLI / Compiler Directives	
	Day 2								
	Day 3							Revise - HDL	Revise - HDL
	Day 4							Revise - HDL	Test - HDlL
Environments	Day 5	EDA tools	Practical - Tools	Lab - Frontend Design & Verification		Lab - Frontend Design & Verification		Demo - Frontend Design & Verification	
				Mini Project		Mini Project			
Environments	Day 6	EDA tools	Practical - Tools	Lab - Frontend Design & Verification		Lab - Frontend Design & Verification		Check Point Results & Counselling	

	Month 3							
	Day	Week 1		Week 2		Week 3		Week 4	
		10:30 - 12:30	6:00 - 8:00 pm	10:30 - 12:30	6:00 - 8:00 pm	10:30 - 12:30	6:00 - 8:00 pm	10:30 - 12:30	6:00 - 8:00 pm
Logic Design	Day 1	Methodologies IP, FPGA, ASIC & SOC		VDL - Advanced - SystemVerilog		VDL - Advanced - SystemVerilog		Adv Verification Methodologies - OVM	
	Day 2								
	Day 3	OOPS						Revise - Methodologies	Revise - SystemVerilog
	Day 4							Test - Adv Method	Test - Methods & VDLs
Environments	Day 5	Paper Writing	Paper Writing	Lab - VIP		Lab - VIP		Lab - VIP	
Environments	Day 6	Paper Writing	Presentations-Paper	Lab - VIP		Lab - VIP		Lab - VIP	Demo - eVc or VIP

	Month 4							
	Day	Week 1		Week 2		Week 3		Week 4	
		10:30 - 12:30	6:00 - 8:00 pm	10:30 - 12:30	6:00 - 8:00 pm	10:30 - 12:30	6:00 - 8:00 pm	10:30 - 12:30	6:00 - 8:00 pm
Logic Design	Day 1	Hosts - PCI		Processor - Verification		Backend - Semi-custom - STA		Backend - Full Custom	
	Day 2								
	Day 3	Data Comm - USB		Backend - Static Timing Analysis				Rev Host & Data & Proc	Test - Host, Etc
	Day 4							Rev - Backend	Test - Backend
Environments	Day 5	Presentation Writing		Lab - Semi Custom		Lab - Semi Custom		Demo-Semi Custom	
Environments	Day 6	Presentations - Prep	Presentations	Lab - Semi Custom		Lab - Semi Custom		Check Point FINAL Results!	