Factsheet

SafeSPI Protocol®

Silicon Cores™

Core to the Intelligent System™

Function Controller

Silicon Interfaces' SafeSPI is a secure version of the SPI protocol that has been designed to provide enhanced security features, making it suitable for use in sensitive applications. Error detection through the SPI is crucial in ensuring the safety and reliability of airplanes. The SafeSPI protocol ensures that all data transfer is performed securely, preventing any unauthorized access to the transmitted data.

- **SafeSPI** support CRC (Cyclic Redundancy Check).
- **SafeSPI** provides the capability to transfer the data in packet format.
- **SafeSPI** supports backdoor access for memory and registers.
- **SafeSPI** supports bit encodings.

Cyclic Redundancy Check, is a common method used in SPI communication to verify the integrity of data transmitted between the master and slave devices. It is a type of checksum calculated by the transmitter over a specific portion of the data.

SafeSPI, the master and peripheral devices exchange a set of cryptographic keys during the initialization phase, which is used to encrypt and authenticate the data transmitted between them. This ensures that only authorized devices can participate in the communication and that the data exchanged is not modified or tampered with during the transmission.

Product Specifications

- Fully synthesizable Register Transfer Level (RTL) Verilog HDL core.
- Test Bench. (Environment Variable: UVM)
- Targeted FPGA Xilinx Series 7 FPGA
- Clock Frequency: IP core clocks are adjustable (60 MHz for internal)
- Standard IO

Options:

(May be separately priced)

Adaptations:

√ Dual-SafeSPI two data lines are available for data transfer

√ 8/64-Bit Standard Microcontroller Interface possible

Add-ons:

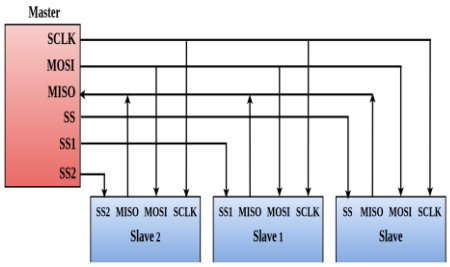
√ Verification IP – UVM VIP

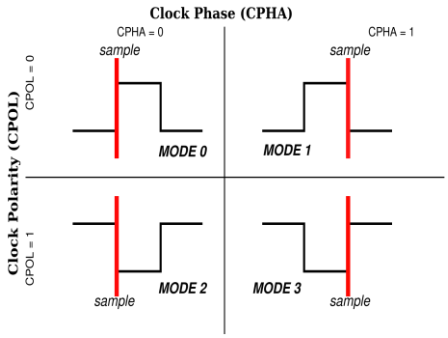
SafeSPI requires the selection of a specific SPI mode, which is determined by the clock polarity (CPOL) and clock phase (CPHA) settings. These settings dictate when data is latched and shifted, as well as the edges of the clock signal that trigger these actions. By carefully selecting the appropriate CPOL and

SPI Mode	Clock Polarity	Clock Phase	Data is Latched at	Data is shifted at
0	0	0	Rising Edge	Falling Edge
1	0	1	Falling Edge	Rising Edge
2	1	0	Rising Edge	Falling Edge
3	1	1	Falling Edge	Rising Edge

Product Highlights

- ☑ Full-duplex Serial communication
- ☑ 48Bit and 32Bit support in the same Slave.
- ☑ Sensor time critical response.
- ☑ SafeSPI supports CRC for verifying the integrity of data transmission.
- ☑ SafeSPI provides secure and robust communication
- ☑ Analogue-to-Digital converts and Digital-to-Analog converts can use SPI to transfer data from the microcontroller
- ☑ SafeSPI is support 32-bit and 48-bit in-the-frame and out-of-frame data formats.
- ☑ SafeSPI clock frequency depends on a variety of factors.





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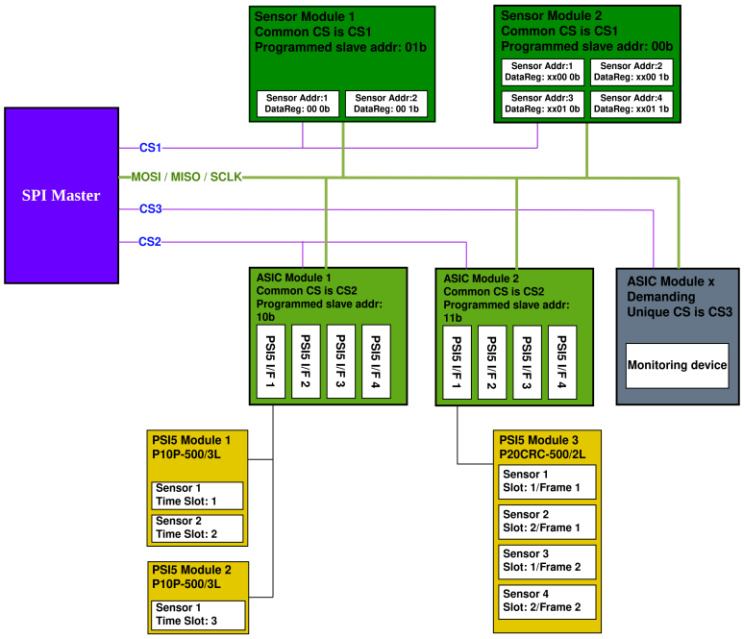
SafeSPI Block Representative



The SafeSPI function core consists of four main modules: SafeSPI interface, SafeSPI master module, SafeSPI slave module, and SafeSPI top module.

- SafeSPI Interface: In the SafeSPI module, the top-level signals are declared in the interface, and their direction is defined in the modport to ensure proper synchronization and avoid race conditions between the master and slave modules. By carefully specifying the direction of each signal, the master and slave can communicate with each other safely and reliably. This helps to prevent conflicts and ensure that the SPI protocol is executed correctly.
- SafeSPI Master: The SafeSPI module contains a struct that defines the master's data, as well as two tasks for handling SPI communication in two different modes of the protocol (0/2 and 1/3). To ensure that the master's data is valid for the selected SPI mode, it is randomized and constrained accordingly. During SPI communication, the master's data is shifted out on the MOSI line, while the MISO line receives data from the slave. The data is shifted either on the positive or negative edge of the SPI clock (SCLK), depending on the selected SPI mode. The SafeSPI tasks monitor the slave select (SS) line, and when it goes low, they initiate SPI communication by shifting data out on the MOSI line. The tasks continue shifting data until they receive data from the slave, at which point they end the communication by raising the SS line.
- SafeSPI Slave: The SafeSPI module includes two tasks for implementing the slave mode 0/2 and mode 1/3 data transfer protocols, respectively. These tasks use the interface to communicate with the master device and ensure safe and reliable data transfer. To shift the data correctly, the tasks sample the data at the appropriate edge of the SCLK signal and shift the data to the opposite edge. Additionally, they use the "SPI_MASTER" module to verify the received data from the master device, ensuring the integrity of the data transfer.
- SafeSPI Top: The SafeSPI module includes the instantiation of the interface, as well as the master and slave modules. These components interact with each other to facilitate safe and reliable communication between the master and slave devices.

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