Factsheet SI25WLANBBP10

802.11 a b and g IEEE Standard

Silicon Cores™

Core to the Intelligent System™

Wireless LAN (BBP)

Silicon Interfaces' BBP core for Wireless LAN is compatible with 802.11 a b and g IEEE standards. It is designed to handle packetized DSSS (Direct Sequence Spread Spectrum) and OFDM (Orthogonal Frequency Division Multiplexing) data transmissions.

BBP is a PHY entity for an OFDM and DSSS, aimed for data transfer rates upto 54 Mbps at the unlicensed frequency range of 2.4 and 5 GHz. This specification describes the functions of the signal processing in the medium and the interface with the radio.

BBP Core is designed to be used at higher speeds providing maximum performance with minimum power consumption. High decode gain Viterbi algorithm for added performance. The Baseband processor can interface to an RF using either an analog I/Q interface or a digital interface.

Applications:

- Home networking for device sharing.
- Consumers and SOHO applications.
- Wireless multimedia.

Product Specifications

- Fully Synthesizable Register Transfer Level (RTL) VHDL.
- Test Bench Environment: VHDL
- DSP modules done in C language.
- Targeted to Altera Stratix EP1S2

For OFDM:

Data Rates (Mbps)	Modulation Type	Coding Rate	Coded bits per subcarrier
6,9	BPSK	½, ¾	1
12,18	QPSK	½, ¾	2
24, 36	16-QAM	½, ¾	4
48, 54	64-QAM	2/3, ¾	6

For DSSS:

Data Rates (Mbps)	Modulation type
1	DBPSK
2	DQPSK
5.5, 11	CCK

Options:

(May be separately priced)

Adaptations:

√ Nil.

Add-ons:

√ 802.11a/b/g MAC Protocol Available.

Product Highlights

- ☑ Fully Compliant to IEEE 802.11a IEEE 802.11b and IEEE 802.11g PHY layer functions and frames.
- ☑ Interfaces with most existing RF. Compactable with TI RC2436B.
- ☑ Data rates up to 11 Mbit/sec (802.11b) and 54 Mbit/sec (802.11a and 802.11g).
- ☑ It is based on the Fast Fourier transform (FFT) concept, which allows the multiple subcarriers to overlap yet maintain their integrity.
- ☑ High throughput data rates are achieved in OFDM due to precise carrier spacing and exact amplitude and phase settings for each individual carrier constellation.
- ☑ Forward Error Correction coding to improve the data relaiability.
- ☑ The sensitivity as well as multi-path tolerance of the BBP is among the best in the industry.
- ☑ Optimized for Low Power Consumption
- ☑ Optimum hardware-software partitioning for reduced gate count as well as lower MIPS requirements.

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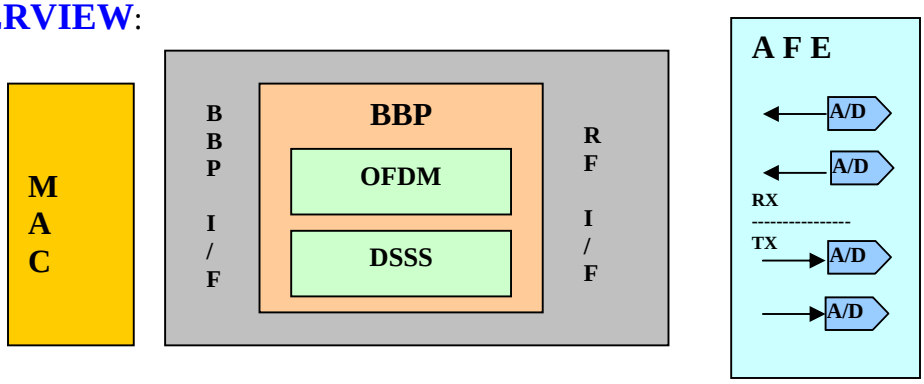
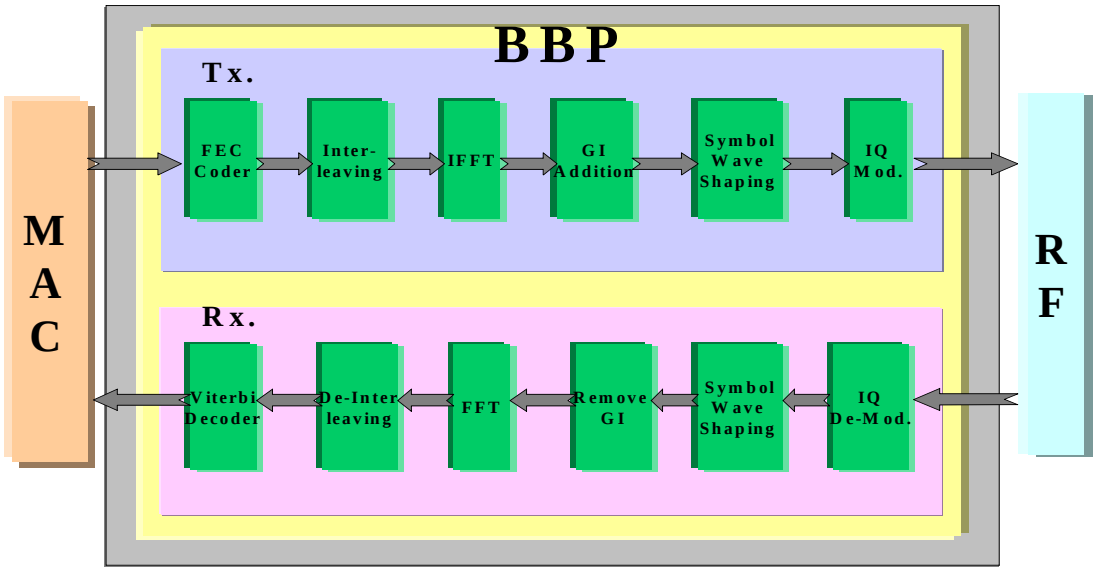
BBP OVERVIEW:



BaseBand Processor Block Representative Schematic:



Brief description of BBP Modules:

FEC Coder: Type of DSP that improves data reliability by introducing a known structure into a data sequence prior to transmission. These structures enables a receiving system to detect and possibly correct errors caused by corruption from the channel and the receiver.

Interleaving: It is the way of arranging the data in a non-contiguous way, so as to improve the performance.

IFFT: Inverse Fast Fourier Transform is used to create the orthogonal subcarriers in the transmitter. It finds the time domain representation from the frequency domain.

Guard Interval Addition: It is the waiting time, to prevent the multipath errors by transmitting a short block of data (symbol), until all the multipath echoes fade before sending other symbols.

Symbol Wave Shaping: A filter representing the multipath channel shapes the frequency domain of the received signal.

IQ Modulation: The modulation techniques used to produce different data rates depending on the coded rates and coded bits per subcarrier.

Viterbi Decoder: Using a Viterbi Algorithm for decoding a bit stream that has been encoded using FEC.

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