Factsheet

SI85SCC30

Serial Communications Controller

Silicon Cores™

Core to the Intelligent Network™

Product Features

- Designed for use with 8 and 16-bit microprocessors.
- Reliable operation with 25Mhz clock.
- On-chip crystal clock oscillator, DPLL and Baud Rate Generator.
- Two Independent full-duplex channels.
- Receiver data registers quadruply buffered.
- NRZ, NRZI, FM encoding / decoding.
- Fully synthesizable Register Transfer Level (RTL) VHDL

Synchronous/Isochronous data rates:

- Upto ¼ of the PCLK (2.5 Mbits / sec) maximum data rate with 10 MHz PCLK using external phase locked loop.
- Upto 625 Kbit / sec with a 10 MHz clock rate. Upto 500Kbit / sec with a 8MHz clock rate (FM encoding using DPLL).
- Upto 372.5 Kbit / sec with a 10 MHz clock rate. Upto 250 Kbit / sec with a 8 MHz clock rate (NRZI encoding using DPLL).

Asynchronous Capabilities:

- 5,6,7 or 8 bits per character.
- 1,1-½ or 2 stop bits.
- Odd or Even parity.
- Times 1,16,32 or 64 clock modes.
- Spike rejection mechanism, break generation and detection and also parity overrun and framing error detection.

Synchronous capabilities:

- Internal or external synchronization.
- 5,6,7 or 8 bits per character with 1 or 2 sync characters in separate registers.
- Automatic CRC generation (CRC-16 / SDLC- CRC) generation / detection.

SDLC/HDLC Capabilities:

- 5,6,7 or 8 bits per character.
- Abort sequence generation and checking.
- Automatic zero insertion / deletion and detection.
- Automatic flag insertion between messages.
- Address field recognition.
- SDLC Loop-mode with EOP recognition / loop entry and exit.
- CRC-16 / SDLC-CRC generation / detection.

Serial Communication Controller

SI85CC30

The SI85SCC30 SCC is a dual channel, multiprotocol data communications peripheral. It supports virtually any serial data transfer application with important functions like baud rate generator, digital phase locked loop on the cell, it makes a self contained controller. In proportion to its functionalities the pin count is very less

Architectural Overview

The SCC internal architecture includes two full duplex channels, two baud rate generators, internal control and interrupt logic, and a bus interface to a non multiplexed bus. Associated with each channel are a number of read and write registers for mode control and status information, as well as logic necessary to interface to modems or other external devices.

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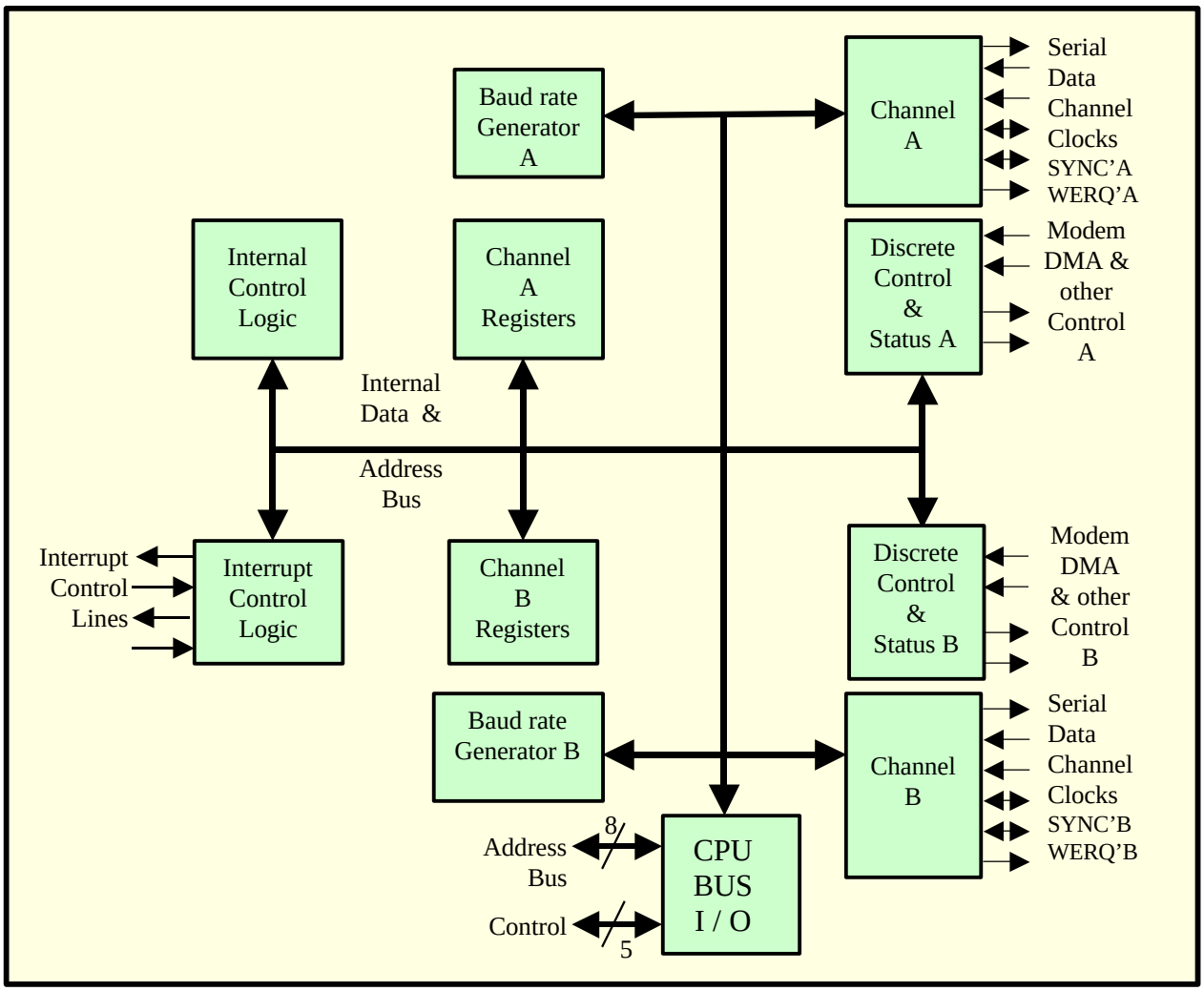
Serial Communication Controller Block Representative Schematic:



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