Factsheet

GEMAC OVC SI80GEOVC10

Silicon Cores™

Core to the Intelligent System™

Gigabit Ethernet MAC SystemVerilog OVC VIP

Gigabit Ethernet Media Access Control (MAC) SystemVerilog OVC VIP is fully documented, off-the-shelf component for the developers of the Gigabit Ethernet MAC. Full Programmability and versatility of the OVC enables connection to any standard IEEE 802.3 based GEMAC device and supports application of Stimulus to the generic microcontroller Interface as well as PHY Interface

The GEMAC OVC based VIP provides a concise, declarative mechanism to code the specification of sequences of events and activities of Gigabit Ethernet MAC Protocol. This methodology provides the best framework to achieve coverage driven verification.

GEMAC VIP is developed using the OVM Class Library that includes ovm_sequence, ovm_driver etc. base classes and capabilities to create modular, reusable components. This methodology combines automatic test generation, self-checking test benches and coverage metrics to significantly reduce the time spent verifying a design under test.

Silicon Interfaces' GEMAC core implements the Ethernet Media Access Control (MAC) protocol according to IEEE 802.3 specification. The MAC has a standard Gigabit Media Independent Interface (GMII) to connect to any PHY interface. A single channel MAC with PCI controller would provide an ideal solution for inexpensive NIC cards.

Product Specifications

- The OVM VIP can be adapted to test a standard Gigabit Ethernet MAC device in a Verification environment
- Separate set of tasks provided for Transmit as well as Receive sections in Full-duplex mode
- Extensive checking of the PHY Interface for the MAC

Product Highlights

- ☑ Fully OVM-compliant and completely configurable with SystemVerilog environment, as per user requirements and OVM user guide for OVC's.
- ☑ Accurately verifies IEEE 802.3 standard Gigabit Ethernet MAC specifications
- ☑ Application of Stimulus to the Generic Microcontroller Interface as well as PHY Interface
- ☑ OVM based transactions using monitors, checkers and scoreboards.
- ☑ Supports scoreboard checking
- ☑ Built in Coverage model implemented for all transaction types
- ☑ Built in Monitors for protocol monitoring and checking
- ☑ Provides checking of valid Inter Packet Gap
- ☑ Support for checking of normal as well as VLAN tagged Packets
- ☑ Supports checking of Pause Frames
- ☑ Provides Checkers for Minimum and Maximum payload sizes, for both normal as well as VLAN tagged Packets
- ☑ Checkers to determine validity of Preamble bits along with SFD
- ☑ Separate Configuration file for Parameter definitions

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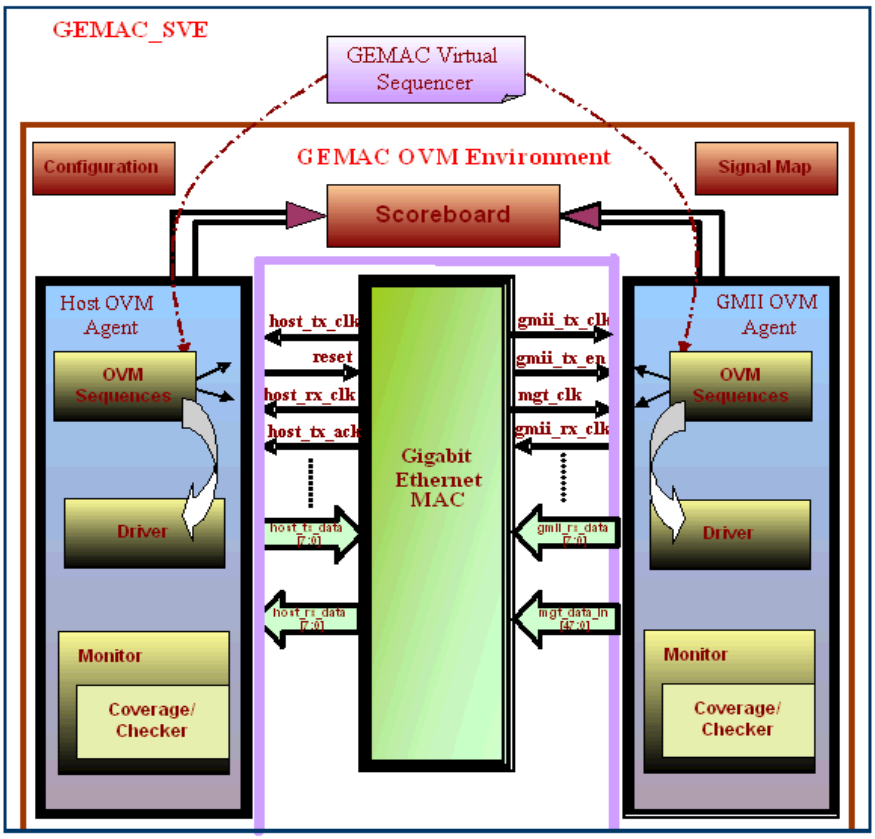
GEMAC OVM Environment



GEMAC DUT Description:

The **Gigabit Ethernet MAC** is connected between the Microcontroller-based **Host** and Physical Layer. The Microcontroller serves as the Host (Link Layer), which receives and transmits Packets from and to the **MAC**. The other end of the **MAC** is connected to the **PHY** (Physical Layer).

The **OVC VIP** is built around the **DUT** as an epicenter. Constructs within monitor the interfaces and provide a detailed log on the transactions that take place to and from the **DUT**. Thus, just by looking for Successes or Failures within the log output, the function of the **Gigabit Ethernet MAC** could be easily and effectively validated.

OVM Environment Description:

GEMAC Virtual Sequencer has collection of OVM based virtual sequences to control **Host** as well as **GMII** sequences. Sequences are the stimulus data which is fed to the **DUT** through the **Driver**. The **OVC Class Library** provides the **ovm_sequence** base class. These sequences are derived from the base class. The sequences body tasks are implemented with the specific scenarios to execute the sequences.

The **Driver** obtains data items from the sequencer for execution. The driver's role is to drive data items to the bus following the interface protocol. The **Driver** classes are derived from the **ovm_driver** base class.

Monitor extracts signal information from the bus and translates it into events, structs, and status information. The **Monitor** functionality includes protocol checking and coverage collection.

A **Scoreboard** verifies the proper operation of the design at a functional level. It taps the information going in and out of the **DUT** and determines the **DUT** response according to the stimulus generated.

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