

Factsheet

IEEE 1394 OVC - SI170FWAOVC11

OVM Based IEEE 1394 Link Layer Controller OVC Verification IP

Silicon Interfaces' 1394 OVC is a fully documented, off-the-shelf component using the Open Verification Methodology for quickly enabling functional verification. The OVM based application programming interface (API) supports the IEEE standards of both SystemVerilog and e, enabling the powerful combination of field-proven verification capabilities, a multi-language interface, and scaleable OVM methodology.

The OVM-compliant 1394 OVC supports IEEE 1394 PHY specification at the Physical side (PHY side) and Transaction Layer specification at the Host side. Data transmission can be configured with different speeds (100, 200 or 400 Mbps) and can be configured with different transfers (Asynchronous or Isochronous transactions).

The 1394 Function Controller OVM-compliant OVC verifies designs that conforms to standard IEEE 1394 specifications. The 1394 OVC consists of a complete set of verification capabilities like sequencer, checker, coverage metrics and SystemVerilog API interfaces within the OVM. The 1394 OVC combines built-in coverage analysis, self-checking test benches and coverage metrics to significantly reduce the time spent verifying a design under test.

The 1394 OVC test bench is composed of reusable verification environments called universal verification components (UVCs). A UVC is an encapsulated, ready-to-use, configurable verification environment for an interface protocol, a design sub-module, or a full system.

Silicon Interfaces' 1394a-2000 Link Layer Controller Core provides data packet delivery service for Asynchronous and Isochronous (real-time) data transmission. It performs arbitration request, packet generation and checking as well as data acknowledgement transmission.

Silicon Cores™

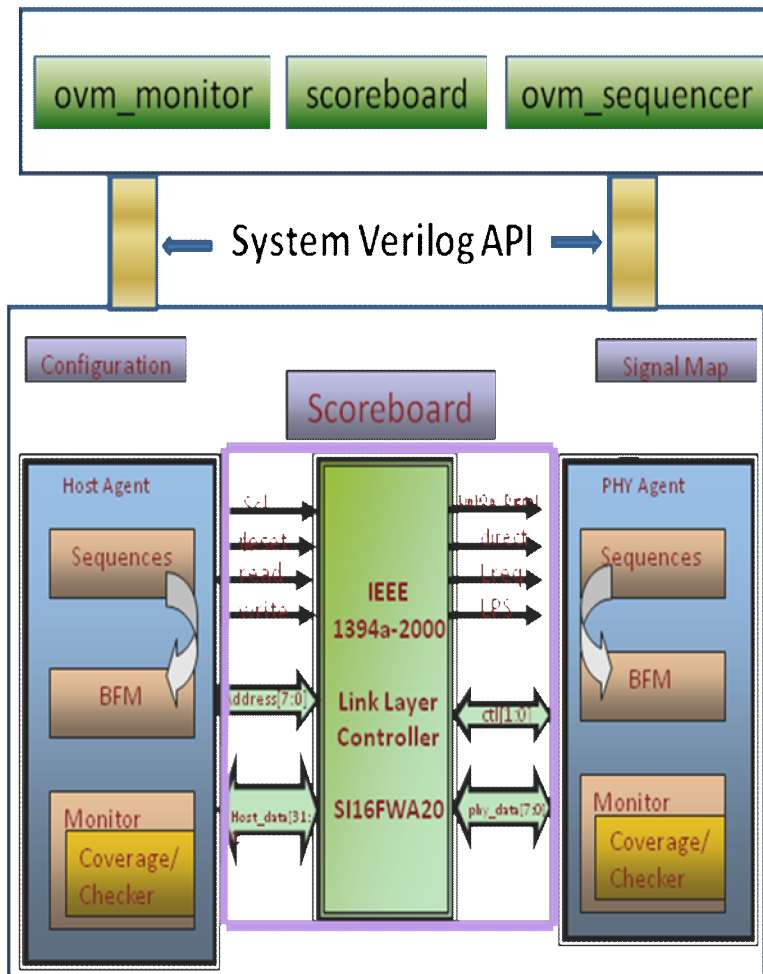
Core to the Intelligent System™



Product Highlights

- ☑ Fully OVM-compliant and completely configurable with SystemVerilog or e environment, as per user requirements and the OVM User Guide for OVC's
- ☑ Fully compliant with the IEEE 1394 specifications
- ☑ Support data rates at 100 Mbps, 200Mbps and 400 Mbps
- ☑ Supports IEEE 1394 PHY interface at Physical side and Application, Transaction layer and Serial Bus Manager features at the Host side.
- ☑ Supports protocol monitoring and checking through both phy and host monitors using OVM-compliant System Verilog API
- ☑ Supports direct and random stimulus generation using OVM sequencers
- ☑ Built-in coverage analysis for both asynchronous and isochronous transfers using OVM
- ☑ OVM based transactions using monitors, checkers and scoreboards.
- ☑ Supports end-to-end scoreboard checking.
- ☑ Can be configured to be in root and non-root mode to check generation and reception of cycle start packet
- ☑ Computing CRC of data packets & error notification
- ☑ HDL independent.

IEEE 1394 OVM Block Representative Schematic:



Verification Methodology:

An IEEE 1394 Link Layer Controller OVC with OVM compliant System Verilog API, initiates the IEEE 1394 PHY layer, Transaction layer and Application layer compliant transactions. These transactions are applied to the DUT.

The OVM compliant System Verilog API of e-based 1394 Link Layer Controller UVC contains configuration file to define the verification environment, Monitor to serve for adding checks and Sequences to control the test scenarios.

The e based UVC Scoreboard, compares the data collected at the HOST or the PHY Receiver with the data driven from the PHY or HOST Transmitter respectively, thus verifying adherence to the IEEE 1394 Protocol.

The e based UVC Monitor collects data items from the respective HOST or PHY agent interface and e based UVC Coverage module operates based on events and data collected by the Monitor. The Monitor, Scoreboard and Coverage is enhanced with OVM UVC components.

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