Factsheet
Gigabit – SI50GE22

Silicon Cores™
Core to the Intelligent System™

Gigabit Ethernet MAC

Silicon Interfaces' **Gigabit Ethernet Media Access Controller is highly integrated Gigabit Ethernet MAC solution for Gigabit applications. It simplifies design of Gigabit systems and reduces time-to-market. It is also a companion device for any Network Processor and enables glueless Gigabit Ethernet backbone connectivity.**

The GEMAC (Gigabit Ethernet Media Access Controller) core implements the Ethernet Media Access Control (MAC) protocol according to IEEE 802.3 specification. The MAC has a standard Gigabit Media Independent Interface (GMII) to connect to any PHY interface. The core can be used in various integrated applications. A single channel MAC with PCI controller would provide an ideal solution for inexpensive NIC cards.

The complete modular design of the cores facilitates easy customization to include value added and distinguishing features.

The GEMAC implements half duplex functions such as Carrier Extension and Packet Bursting. In full duplex mode, the GEMAC implements both symmetrical and asymmetrical flow control via IEEE 802.3x Pause MAC Control frames. Pause frames can be generated according to flow control thresholds within the

Product Specifications

- Fully synthesizable Register Transfer Level (RTL) Verilog HDL core.
- Fully functionally verified core. (Verilog)
- Targeted to ASIC (TSMC (0.15, 0.18 and 0.2 micron))
- Standard GMII Physical Interface
- Clock Frequency: 130MHz (TSMC)

Options:

(May be separately priced)

Adaptations:

√ 32 bit PCI Host Interface (PCI MAC) - available
√ 64 Kbyte (Max) Transmit and 64 Kbyte (Max) Receive External Buffer Memory Interface in place of Internal FIFO – available
√ Powerful statistics database Management Information Database (MIB based on RFC2665) providing information to external user or management object – available
√ IEEE 802.1q VLAN compliant – available
√ Configurable Jumbo frames of any length – available
√ Programmable inter-frame gap adjustment – available
√ Capable of loop-back diagnosis mode – available
√ Supports 802.3ad Link Aggregation and 802.ac Tagging – available
√ Supports Ten Bit Interface (TBI) – available
√ Supports IEEE 802.3-2002 specification

Add-ons:

√ 16-bit MII (Media Independent Interface) - available
√ RMII (6 pin Reduced MII) - available
√ PCS Interface physical layer attachment (PMA) for 1000Base-X (i.e. 8b / 10b encoding / decoding and SERDES for transmission / reception) available
√ SMII (2 pin Serial MII) Interface possible

Product Highlights

☑ Highly Integrated Gigabit Ethernet Media Access Controller (MAC) core
☑ Compliance with IEEE 802.3-2000 specifications
☑ Backward Compatible with 100 / 10 Mbits.
☑ Network data bandwidth: 1 Gbps in CSMA / CD (Half Duplex) and 2 Gbps in Full Duplex.
☑ Generic Host Interface
☑ Configurable flow control with MAC control pause frames compliant to IEEE 802.3x for frame-based flow control
☑ Reconciliation Physical Sub-layer with GMII included
☑ 8K Receive FIFO and 4K Transmit FIFO
☑ Carrier Extension and Packet Bursting
☑ Supports 802.3z, Gigabit Ethernet over optical fibres
☑ Supports 802.3ab, Gigabit Ethernet over copper
☑ Supports 802.3u 100 Mbits Fast Ethernet
☑ 2 Independent Clock Domains

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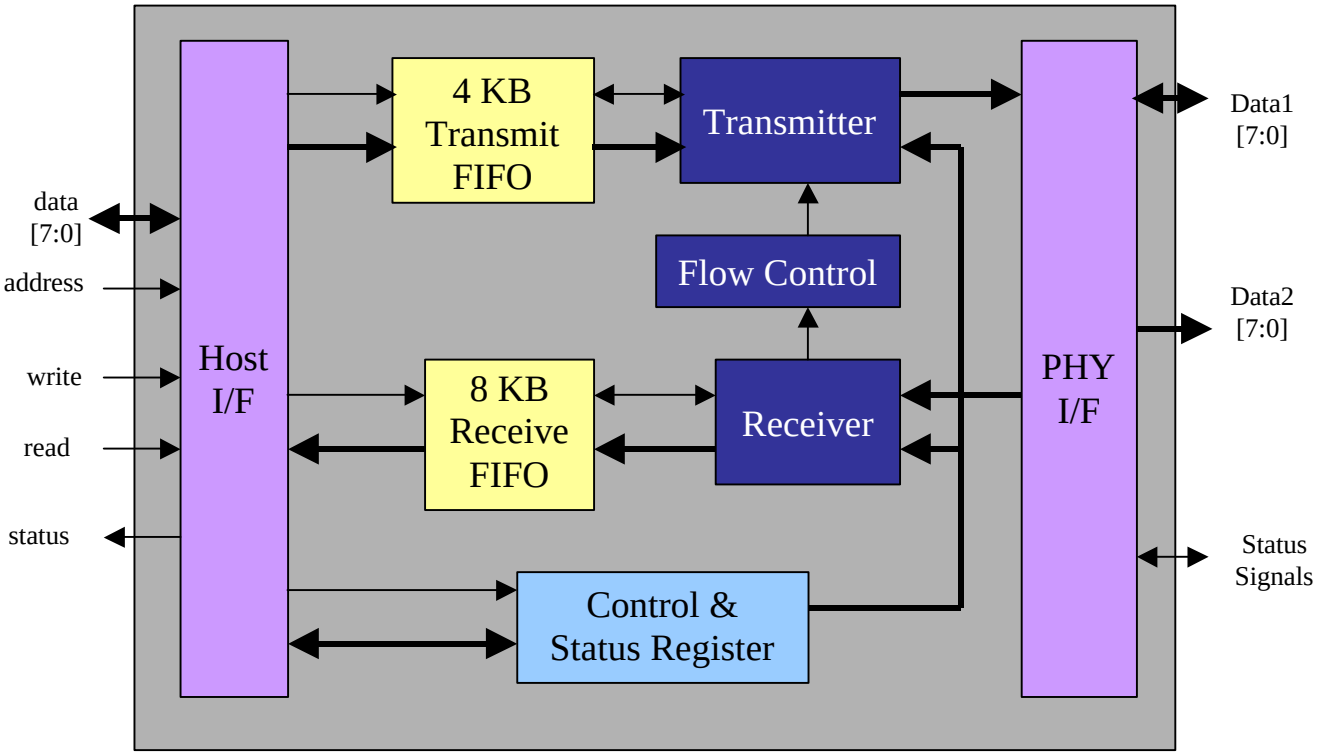
GEMAC Block Representative Schematic:



- Host Interface: The host Interface allows the SI50GE22 to be easily connected to the most 8 bit host processors. The host interface consists of 8-bit data bus and an 8-bit address bus.
- Physical Interface: The physical (PHY) Interface provides a standard Gigabit media independent interface (GMII) to the physical layer
- Transmit and receive fifo: The transmit and receive memory is a 4K and 8K Bytes of internal buffer provided to store the transmitted data and the received data.
- Control and Status Register: The Control and Status Register store the vital information desirable for the proper working of the core. It also stores the status of discarded packets while transmission and reception.
- Transmitter: The transmitter retrieves data from the transmit memory and creates correctly formatted packet to be transmitted through the PHY interface.
- Receiver: The receiver takes incoming data from the PHY interface, checks the validity and stores the valid data into the receive memory or stores the status of the received corrupt packet into the CSR.

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