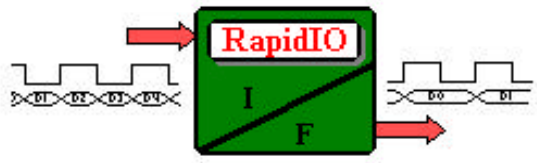
Factsheet

RapidIO™ - SI11RI10

Silicon Cores™

Core to the Intelligent System™

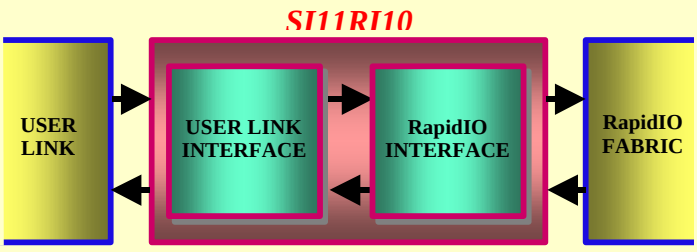


Physical Layer Interface Core

Silicon Interfaces® **RapidIO™ is a packet-switched interconnect intended primarily as an intra-system interfaces for a chip-to-chip and board-to-board communications at Gigabyte-per-second performance levels. Developed as an open standard, the RapidIO™ architecture addresses the needs of present and future systems. RapidIO™ is focused as a processor, memory and memory mapped I/O interfaces optimized for use inside the chassis.**

This high performance low pin-count packet switched system level interconnect provides highly reliable error handling scheme whilst transferring packets between processing elements via the RapidIO™ Fabric.

In the diagram below, the User Application sends data in chunks of 32 bits to the core, which composes and queues the packets in the RapidIO™ format, before transmission to the Fabric. Similarly, the Fabric sends RapidIO™ packets to the chip, which in turn queues and sends data to the User Application via a Microcontroller Interface.



Interface Schematic for Physical Layer Interface Core

Product Specifications

- Fully synthesizable Register Transfer Level (RTL) Verilog HDL core
- Test Bench Environment: Verilog
- Targeted FPGA Xilinx Virtex-II Family
- Clock Frequency: 62.5-125 MHz
- LP-LVDS Buffers (for Fabric end interface)

Options:

(May be separately priced)

Adaptations:

√ 16/32-bit PCI or AMBA Host Interface Possible.

√ AMBA Possible.

Add-ons:

√ NIL

Product Highlights

- ☑ Fully Compliant with **RapidIO™ Interconnect Specification Rev 1.1, 3/2001** prescribed by **RapidIO™ Trade Association**.
- ☑ 32-bit standard Host/Link Interface.
- ☑ **Full Duplex** Independent Transmit and Receive Data Path.
- ☑ Dual Data Rate (DDR): 62.5-125 MHz.
- ☑ Auto scaling 8/16 bit Ports.
- ☑ Respects 32-bit boundaries.
- ☑ **Rx Queuing**: 16 X 128 X 32 or 8 Kbytes of internal buffer.
- ☑ **Tx Queuing**: 8 X 128 X 32 or 4 Kbytes of internal buffer.
- ☑ Maximum Packet Length: 276 bytes.
- ☑ Minimum Packet Length: 8 bytes.
- ☑ Supports a Very Highly Reliable Error Handling Scheme.
- ☑ CRC-16 Polynomial.
- ☑ Incorporates **Intermediate CRC** for Packet Length of 80 bytes or greater.
- ☑ Upto 8 Unacknowledged Packets.
- ☑ 32-Bit Internal Data Path.
- ☑ Supports: **PACKET RERTY**, **PACKET NOT ACCEPTED**, **STOMP**, **TIME-OF-DAY SYNCHRONIZATION**, **TRAINING** and **THROTTLE**.
- ☑ Separate **Management Interface** (CSRs/CARs).
- ☑ Data Rate 250-500 Mbps per LVDS Pin Pair; Upto **8 Gbits per sec** throughput.
- ☑ Outputs 32-bits of Data to User Interface.
- ☑ Full Control of User Interface bus by user.
- ☑ Tx and Rx sections designed for minimum latency between the input and output.
- ☑ **Smart Bandwidth Utilization** (Designed for minimum latency between Link and Fabric, Intelligent EOP avoidance between Back-to-Back Packets).
- ☑ **Fully automated** Test Bench for checking for error-free packets.
- ☑ 3 Clock Domains - 1 for **Management**, 2 for **Fabric** and **Link Interface**.

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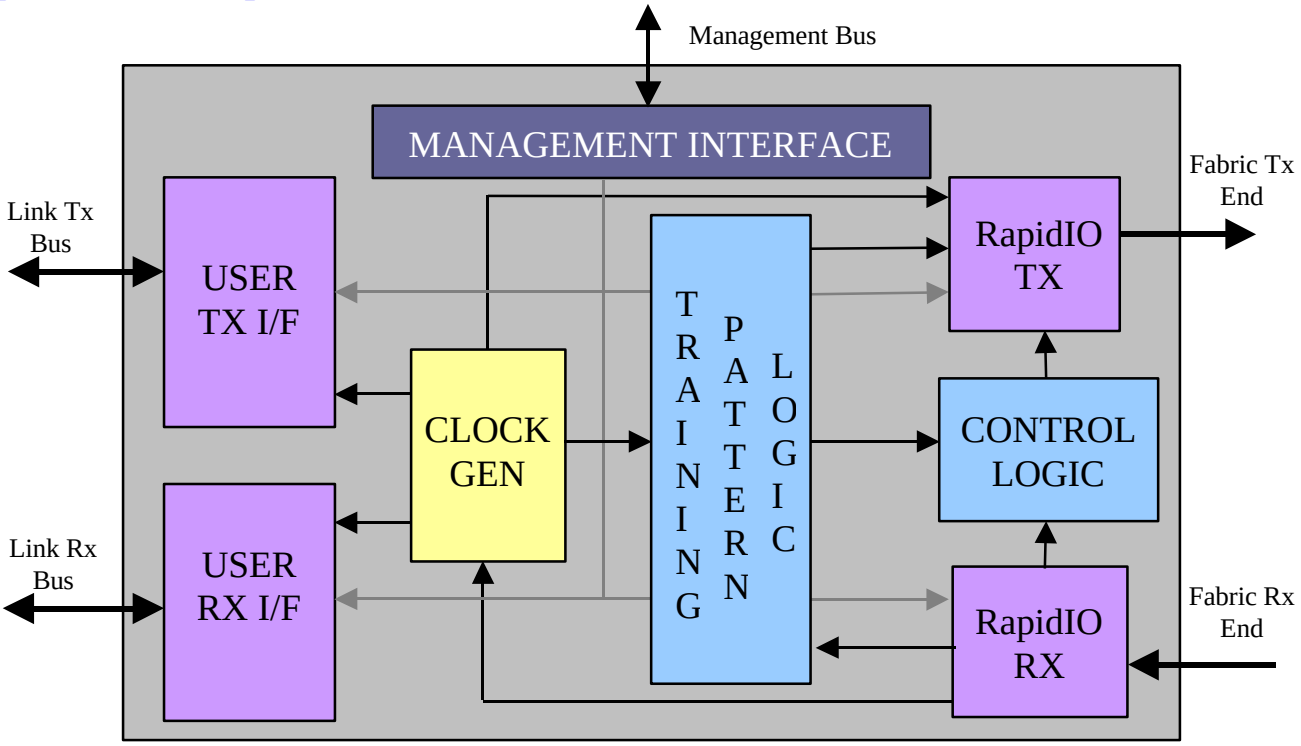
RapidIO Block Representative Schematic:



- **RapidIO RX**: Comprises **Frame Detect** module to detect toggling of **received frame** signal and **CRC-16 Checker** to check the authenticity of received packets**.** The **Receive Buffer Control Logic** controls the transfer of data onto the on-chip **Receive Queue**. The capacity of the Receive Queue is **16 x 128 x 32 bits**.
- **User RX Interface**: It provides Data to **User Link**, which is basically a 32-bit Microcontroller interface.
- **User TX Interface**: Accepts 32 bits of data from the **User Link** and transmits the same to the **Transmit Queue**, which is an on-chip block RAM bearing a capacity of **8 x 128 x 32 bits**.
- **RapidIO TX**: Contains **Transmit Control** logic to pick up data from **TX Queue** and transmit over to **RapidIO™** bus. It also squeezes in **Control Frames** as and when necessary. This section also contains **CRC Generator**, **Transmit Control**, **Transmit Frame Generator** and the **Transmit Queue**. Data from queue is picked up by the **Transmit Control** logic and transmitted over **RapidIO™** Transmit Bus, **tdata [0:31]**, in compliance with **RapidIO™** standard.
- **Control Logic**: This module strips and decodes the various **Control Symbols** transmitted from the **RapidIO™ Fabric**, as well as generates **Control Symbols** to be transmitted over to the **Fabric**.
- **Training Pattern Logic**: This block is responsible for decoding and transmitting **Training Patterns** immediately after chip initialization and as and when required by the adjacent Processing Element across the Fabric. Upon Reset, communication with the Fabric is possible only after the successful completion of the **Training Sequence**.
- **Management Interface**: The **Management Interface** is mainly responsible for writing/reading to/from **CARs** (Capability Registers) and **CSRs** (Command and Status Registers). A totally independent interface has been provided for the same.

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