Factsheet

Silicon Cores™

Core to the Intelligent System™

SONET - SI15SSF01/3

STS-1/3 Framer

***Silicon Interfaces*' STS-1/3 Framer is a single core solution incorporating Synchronous Optical Network / Synchronous Digital Hierarchy (SONET / SDH) protocol as per ANSI and ITU standards. This significantly reduces the cost of implementing complex SONET / SDH System Designs**

SONET / SDH have emerged as significant technologies for building large scale, high speed networks. SONET Multiplexing combines low-speed digital signals such as DS1, DS1C, E1, DS2, and DS3 with required overhead to form a building block called Synchronous Transport Signal (STS-1). The STS-1 operates at the base bandwidth of 51.84 Mbps. The frame rate is 8000 frames per second.

With the STS-1 as a base, higher bandwidths are created using a Time Division Multiplexing (TDM) technology. In this, 3 STS-1s are combined by interleaving a byte from each STS-1 to form an STS-3. The basic frame rate remains 8000 frames per second, but the capacity is tripled to result in a bit rate of 155.52 Mbps. The STS-3 may then be converted to an optical signal (OC-3) for transport, or further multiplexed with three additional STS-3s to form an STS-12 signal, and so on.

Since such high bandwidths are possible with SONET / SDH systems, these systems are widely used in the Internet and large enterprise data networks. Applications include: Video, FDDI, Broadband ISDN, ATM, MPEG-2, in addition to existing DS3 and DS1 services.

Another advantage of SONET is that the Operations, Administration, Maintenance, and Provisioning (OAM&P) capabilities are built directly into the signal overhead to allow maintenance of the network from one central location.

The SONET / SDH Standard allows the interconnection of different manufacturers' optical equipment based on a hierarchy of digital rates, all formed by the interleaving of the basic rate signal – the STS-1. This technology promises to satisfy the bandwidth needs of the world for many years to come.

Product Specifications

- Fully synthesizable Register Transfer Level (RTL) Verilog HDL Core.
- Test Bench (Environment Variable: Verilog)
- Targeted FPGA Xilinx Virtex (2V250fg256) for STS-1

Options:

(May be separately priced)

Adaptations:

✓ Implements the SONET/SDH as per ANSI T1-105, 1995 and ITU-G.707, 1996 specifications.

Add-ons:

✓ STS-3 Framer Available. Full-custom Layout possible.

Product Highlights

☑ Single Core SONET STS-1/3TS-3 Framer Interface giving bandwidth of 51.84 / 155.52 Mbps.

☑ Provides access to internal registers through a Control Interface.

☑ Performs Byte & Frame alignment on the Receive signal.

☑ Generates Frame Co-ordinates (N, row, column) for path processing. Accepts external synchronization pulse for the transmit start of frame.

☑ Inserts the Framing Bytes (A1,A2) and Section Trace J0 Byte or STS-1 ID (C1).

☑ Optionally inserts the section & line data communication channels (D1-D3) or (D4 – D12)

☑ Optionally inserts register programmable APS Byte failure (K1,K2) and synchronization status S1 Bytes.

☑ Computes & inserts section BIP-8 (B1), line BIP-8 (B2), path BIP-8 (B3) and Path Far End Block Error FEBE (G1).

☑ Optionally scrambles the Transmit Frame data and optionally descrambles the receive frame data.

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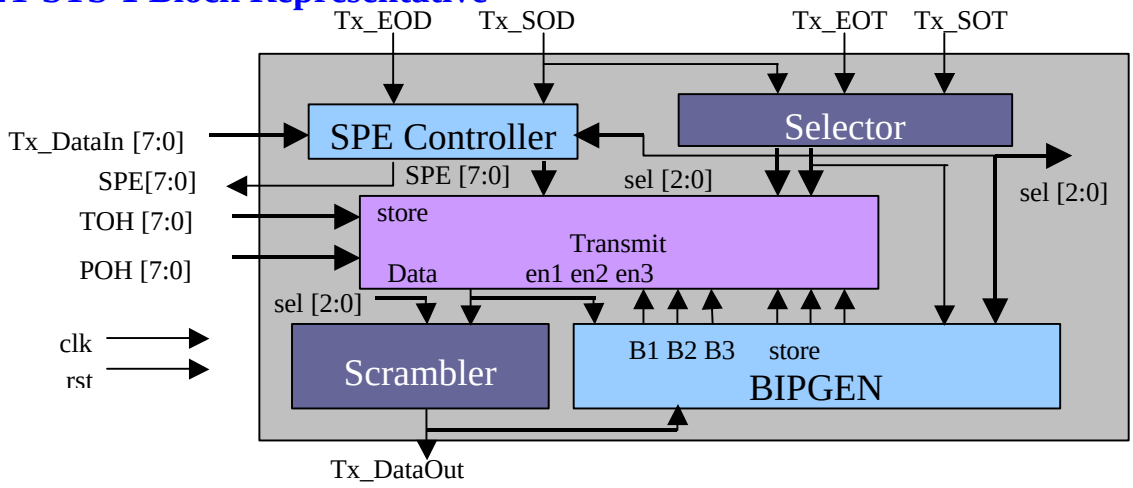
SONET STS-1 Block Representative



BIPGEN: This module is responsible for the generation of Bit Interleaved parity bits for the section, Line and path overhead.

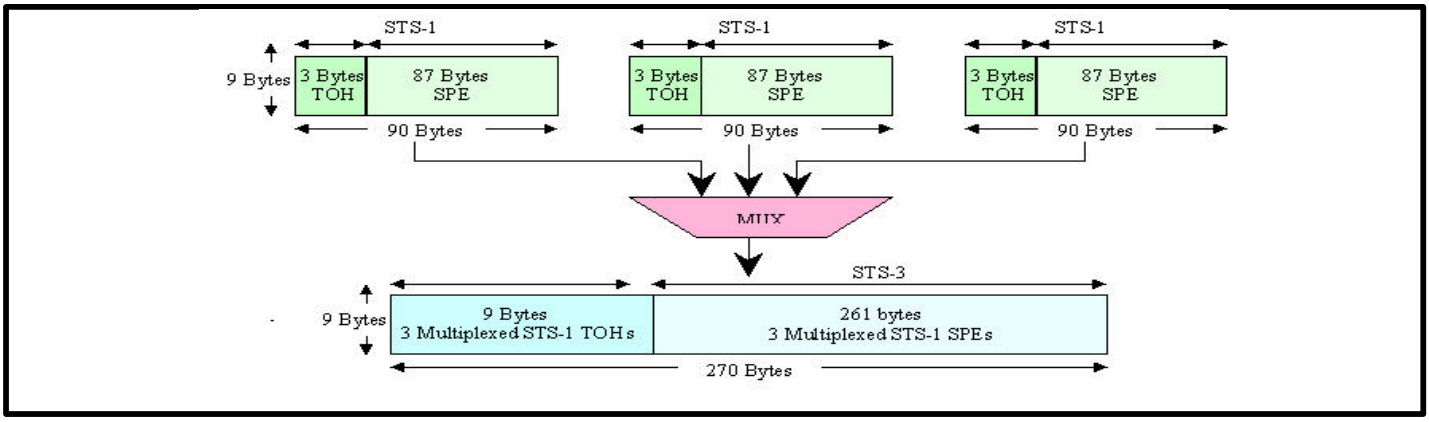
Scrambler: This module is responsible for scrambling the data before it is transmitted on the output line. Scrambling is required for randomisation of data.

Selector: This module is responsible for generating the control signal based on which the framing is done.

SPE Controller: This module is required to control the input i.e. raw data which will be used to form the spe part of the STS-1 frame.

Transmit: This is a multiplexer which selects the source of data which will be transmitted on the data line. It selects the source depending on its select line.

SONET STS-3 Block Representative Schematic:



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