Factsheet

SI40UART01

Universal Asynchronous Receiver/Transmitter Core

Silicon Cores™

Core to the Intelligent Network™

The SI40U550 IP core is a Universal Asynchronous Receiver Transmitter fully compatible with the de-facto standard 16550 UART.

The SI40U550 core performs serial-to-parallel conversions on data received from a peripheral device or modem and parallel-to-serial conversion on data received from the host . The host can read the UART status at any time. The SI40U550 core includes complete modem control capability and a processor interrupt system that can be tailored to minimize software management of the communications link.

The core provides a full-featured transmitter-receiver pair, configurable by software for different speeds, character widths, parity etc. The receiver provides information status with several error indications.

The core can be placed in an alternate FIFO mode. This relieves the CPU of excessive software overhead by buffering received and transmitted characters. The receiver and transmitter FIFOs store up to 16 bytes including three additional bits of error status per byte for the receiver FIFO. In the FIFO mode, there is a selectable auto flow control feature that can significantly reduce software overload and increase system efficiency by automatically controlling serial data flow using RTS output and CTS input signals.

The SI40U550 core includes a programmable baud rate generator capable of dividing a reference clock by divisors from 1 to 65535 and producing a 16x reference clock for the internal transmitter logic. Provisions are included to use this 16xclock for the receiver logic.

DMA operation is allowed with two output signals that inform the DMA controller about when is new received data available and when the UART is able to accept new data for transmission.

Management of modem control outputs and inputs (with their associated interrupt) is included.

Product Features

- Programmable automated RTS and CTS generation
- In automated CTS mode, CTS controls transmitter
- In automated RTS mode, receive FIFO contents and threshold control RTS
- Fully backward compatible with 16450 UARTs
- In the 16450 mode, Hold and Shift registers eliminate the necessity of precise synchronization between the CPU and serial data
- Programmable aud Rate Generator allows division of any input reference clock by 1 to (216 –1) and generates an internal 16x clock
- Standard asynchronous communication bits (Start, Stop, and Parity) added to or deleted from the serial data stream
- Independent receiver clock input
- Fully prioritized interrupt system controls
- Transmit, Receive, Line Status, and Data Set interrupts independently controlled
- Fully programmable serial interface characteristics:
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even-, Odd-, or No-Parity Bit Generation and Detection
  - 1-, 1 1/2-, or 2-Stop bit generation
  - Baud Generation
- False-start bit detection
- Extensive status reporting capabilities
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for serial link fault isolation
  - Break, Parity, Overrun, and Framing error simulation
- Modem control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Fully synthesizable RTL Level Verilog core

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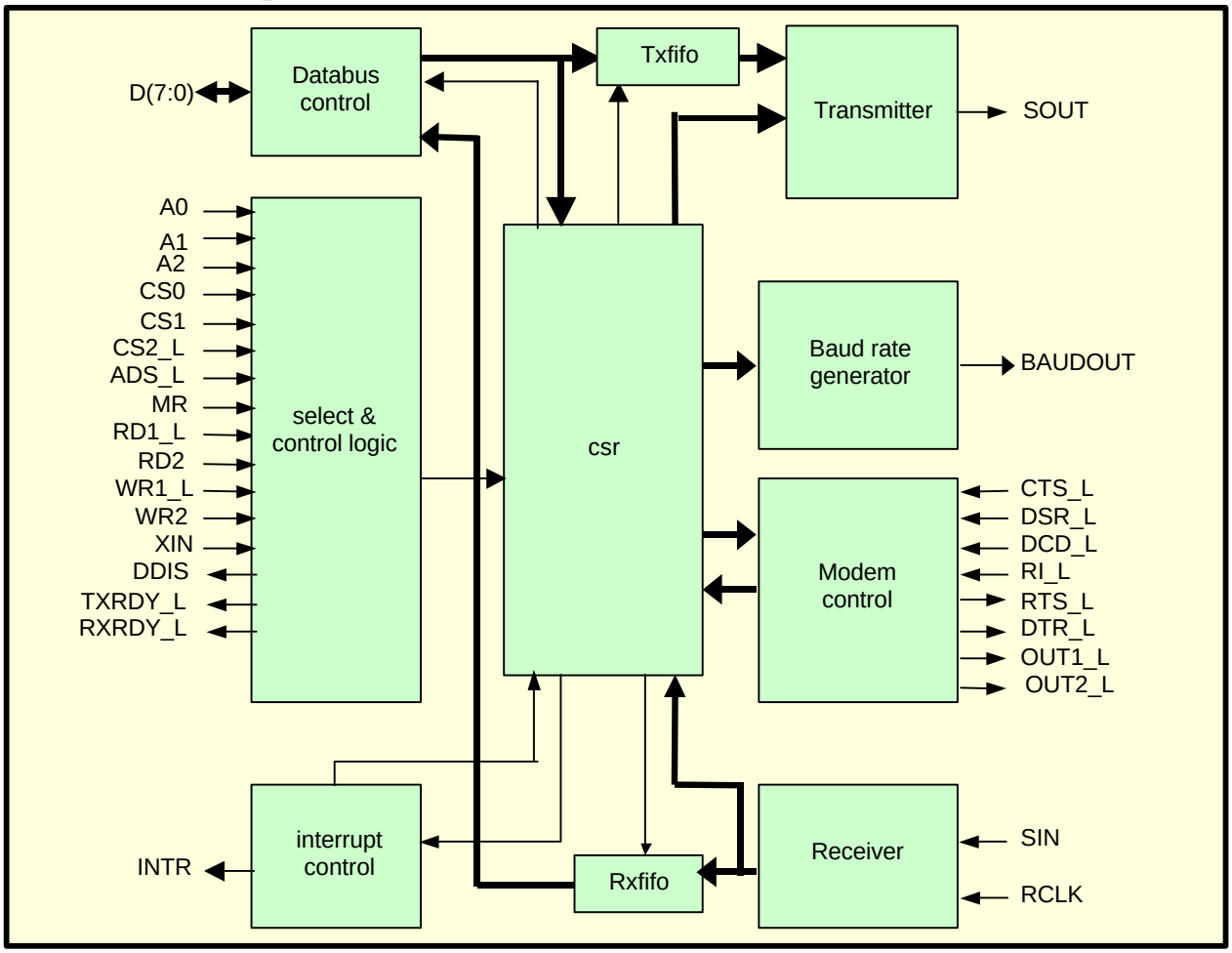
UART Block Representative Schematic:



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