Factsheet

USB2.0® - SI16IB20

Silicon Cores™

Core to the Intelligent System™

Function Controller

***Silicon Interfaces*' USB2.0 function controller is a highly integrated USB solution for USB applications. It simplifies the design of the USB systems and reduces the time to market. The SI16USB20 is a USB Function controller core designed as per USB2.0 revision of USB standards. This core provides 480Mb/s high speed USB interface. It autonomously handles the USB transactions and data transfers, thus bridging the USB interface to an easy read/write parallel interface. It has the standard UTMI interface at host end and a generic microcontroller interface at the device end. It is a is single core solution incorporating USB2.0 protocol operating in Link Layer of Open System Interconnect (OSI) which significantly reduces the time and cost of implementing complex USB2.0 target system designs.**

The Universal Serial Bus (USB) has evolved to the standard interconnect between computers and peripherals. Everything from a mouse to a camera can be connected via USB. With the new USB 2.0 specification, data rates of over 480Mb/s are possible.

The Universal Serial Bus is a point-to-point interface. Multiple peripherals are attached through a HUB to the host.

The rapidly increasing demand for higher interconnection bandwidth is surpassing the performance capacity of existing interconnect devices. USB2.0 is an open architecture that improves data throughput and allows to connect max 127 devices to a single port residing on the PC. USB is a serial protocol and physical link, which transmits all data differentially on a single pair of wires. Another pair provides power to downstream peripherals.

The Universal Serial Bus (USB) was born out of the frustration PC users experience trying to connect an incredibly diverse range of peripherals to their computers. It's the child of vendors whose laptops require a small profile peripheral connector. It further promises to reduce the proliferation of cables and wall transformers that overwhelm even the smallest computer installation. USB is supplanting old-fashioned parallel and serial interfaces in all sorts of applications.

Product Specifications

- Fully synthesizable Register Transfer Level (RTL) Verilog HDL core.
- Test Bench. (Environment Variable: Verilog)
- Targeted FPGA Xilinx Virtex-II (Device: 2V1000bg575)
- Clock Frequency: 79.1MHz for FPGA (Standard: 60 MHz)
- Standard IO

Options:

(May be separately priced)

Adaptations:

√ 8-Bit 8051 Microcontroller Interface

√ 16-Bit Standard Microcontroller Interface possible

√ AMBA possible

Add-ons:

√ Verification IP in OVA (Open Vera Assertion)

Product Highlights

- ☑ Fully compliant with USB2.0 specifications as provided by USB Organisation.
- ☑ Compliance to Test Suites as provided by University of New Hampshire Inter-Operability Lab.
- ☑ Supports High Speed (480 Mbps) Devices.
- ☑ Backward Compatible to USB v1.1 and v1.0
- ☑ Supports Full Speed (12 Mbps) Devices.
- ☑ Supports Low Speed (1.5 Mbps) Devices.
- ☑ Includes Packet Assembler, Packet Disassembler and a Protocol Engine in Protocol Layer.
- ☑ Supports Bulk, Interrupt and Isochronous type transfers.
- ☑ Support for control transfers by endpoint zero.
- ☑ Automatic data entry mechanism.
- ☑ Highly intelligent remote wake-up function.
- ☑ In system Endpoint FIFO – 1 In FIFO or EPIN, 1 Out FIFO or EPOUT and 1 Control FIFO or EPO.
- ☑ EPIN and/or EPOUT may be considered as Bulk or Isochronous or Interrupt Endpoint.
  - Endpoint Buffers are Integrated 4Kbytes on chip data buffer.
- ☑ Endpoints are 8-Bit wide.
- ☑ No Gated Clocks.
- ☑ Support for UTMI v1.03 (USB Transceiver Macro Cell Interface).
- ☑ Generic 8-Bit Microcontroller Interface.
- ☑ Supports 2 Clock Domains; 1 from UTMI and 1 from Microcontroller

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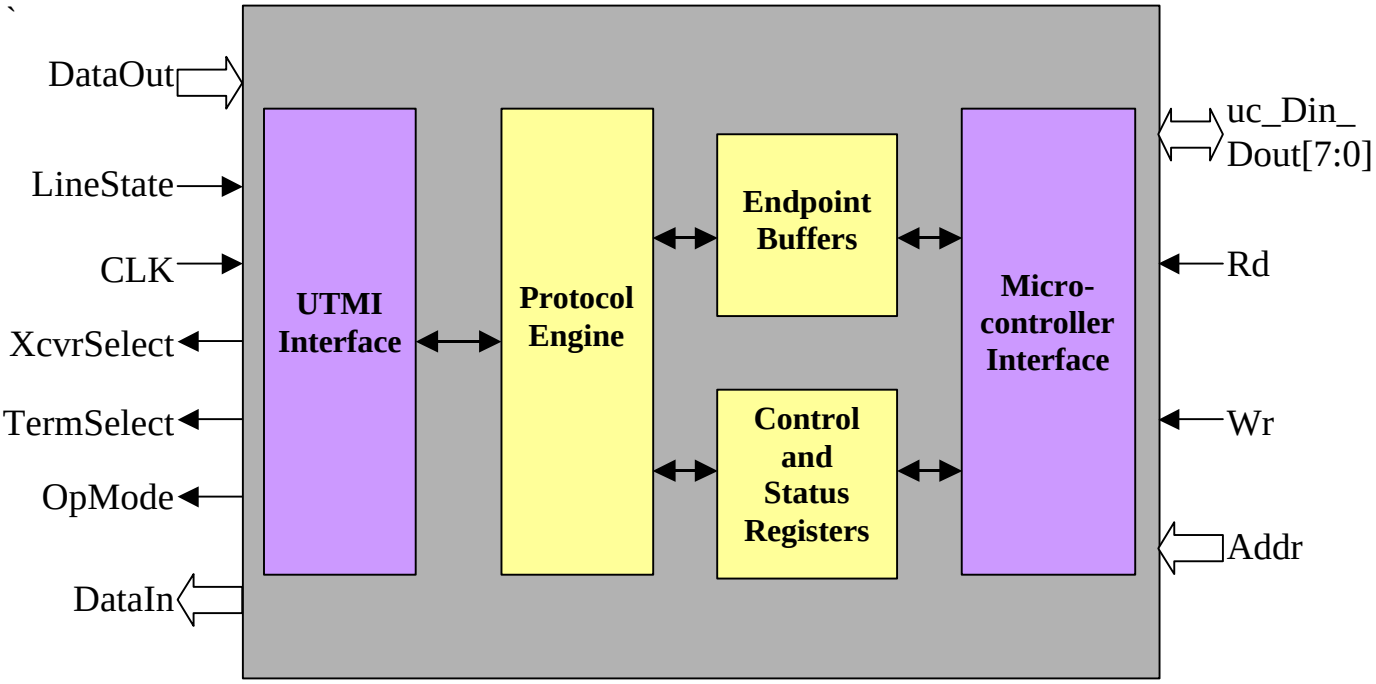
USB Block Representative Schematic:



The USB function core consists of five main modules: UTMI Interface, Protocol Layer (PL), Endpoint Buffers, Control and Status Registers (CSRs) and Microcontroller Interface.

- UTMI Interface: The intent of UTMI (USB tranceiver Macrocell Interface) is to accelerate USB2.0 peripheral development. This interface will enable the IP to be able to design, insulated from the high-speed and analog circuitery issues that are associated with the USB2.0 interface.
- Protocol Layer: PL is the heart of usb function controller. It is responsible for all USB data I/O and control communications. It includes in itself packet assembler, packet disassembler and protocol engine. Packet assembler is responsible for inserting proper pid (packet identifier) and checksums and data field which associates with itself respective crc generation onto that data, if requested. Packet desassembler decodes all incoming packets and forwards the decoded data to the protocol engine and endpoint buffers for further processing. Protocol engine implements standard USB protocol, which includes maintaining the flow of token, data and status paradigm.
- Endpoint: Endpoint buffer is the ultimate source/sink of information. This IP is designed to support 3 endpoints. One is the bi-directional control endpoint used to supply and store configuration related information. Other two endpoints can be configured to support any of the three transfer types interrupt, bulk and isochronous by making one IN and other OUT.
- Control and Status Registers: includes in it information bits which stores the control and status of the current set of operations required by the other blocks.
- Microcontroller Interface: It is used to provide and take signals from the core side and convert those signals in order to be compatible with the microcontroller used on the other side.

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